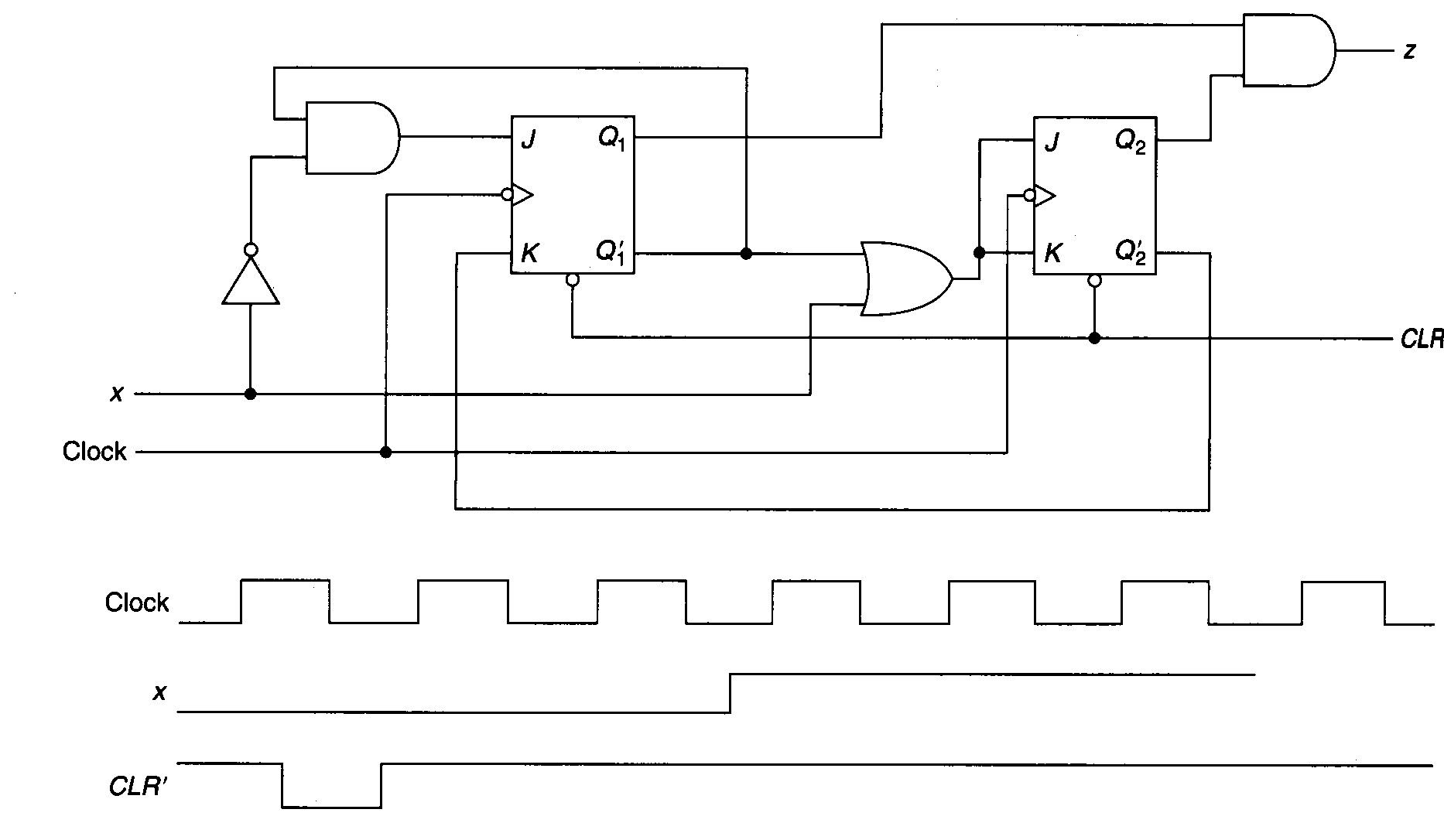
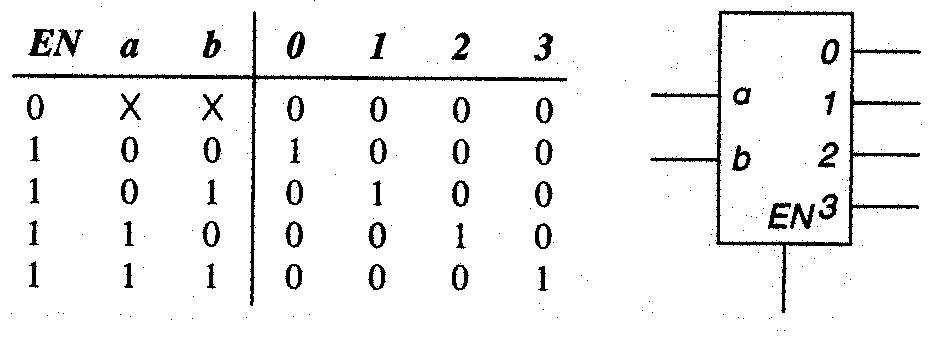
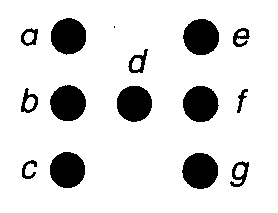
1. For the following circuit, draw the timing diagram of Q1, Q2 and the output z. All flip flops are trailing-edge triggered. Initial value of Q1 and Q2 is zero(15)



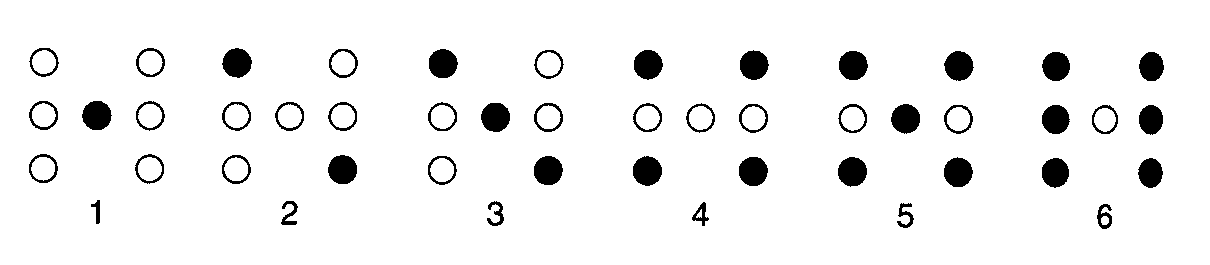
1. Build a 16-way active high decoder, using **only** the four-way decoders shown below. The inputs are x, y, w and z; the outputs are numbered Q0 to Q16. (10)



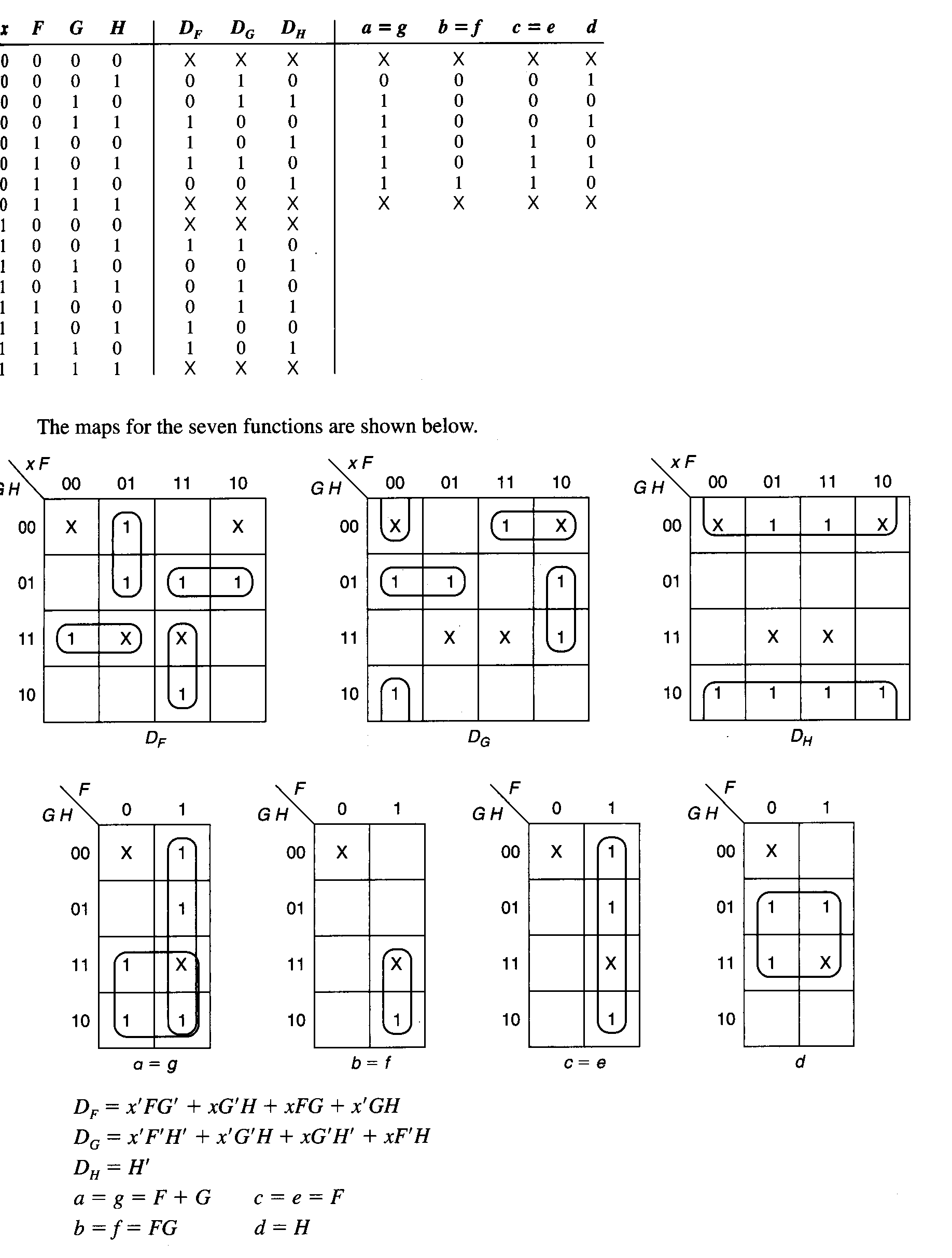
1. Design a system that counts up from 1 to 6 (and repeat) when input X is 0 and down from 6 to 1, when x = 1 and displays the results on a die. The die has seven leds (as shown in the diagram below).



A 1 for each segment (a, b, c, d, e, f, g) indicates that it is lit; a 0 that it is not. The arrangement for the six numbers on a die are shown below, where the darkened circles are to be lit.



Design the counter, using three D flip flops to count from 1 (001) to 6 (110) and repeat. Then, design a decoder/driver that takes the outputs from the counter and produces the seven signals (a, b, c, d, e, f, g) to drive the display. Show state diagram and state table. (25)



1. Construct an Algorithmic State Machine chart for the states A, B and C. The transitions between the state boxes depend on the decisions made by testing the value of the input variable **w**. In each case if w=0, the exit path from a decision box leads to state A. If w=1 then a transition A to B or from B to C takes place. If w=1 in state **C**, then FSM stays in that state. The chart specifies a Moore output z, which is asserted only in state C. In A and B, the value of z is 0 (not asserted). (20)
2. Draw state diagram.
3. Produce state table where the states A, B and C are represented by Y2Y1 = 00, 01 and 10 respectively.
4. Derive a circuit that realizes this state diagram using D flip-flops.
5. Build an 8 output demultiplexer, using **only** the two output demultiplexers.(10)
6. (17)

|  |
| --- |
| For the Algorithmic State Machine chart   1. Type of ASM : M……….. 2. Draw state diagram. 3. Produce state table where the states A and B are represented by X = 0 and 1 respectively. 4. Derive a circuit that realizes this state diagram using D flip-flops. |

1. Design a counter to produce the following sequence : 1 3 0. (15)
2. Use J-K flip flops.
3. Determine the behavior of the circuit in the case of entering unused states.
4. A sequential circuit has two D flip-flops A and B, two inputs x and y, and one output z. For the state diagram chart,(25)
5. Write type of ASM : M………..
6. Draw Algorithmic State Machine chart.
7. Produce state table.
8. Derive a circuit that realizes this state diagram using D flip-flops.

00/0

10/0

11/0

00/1

10/1

11/1

01/1

01/1

10/1

11/1

00/1

01/0

10/0

11/0

00/0

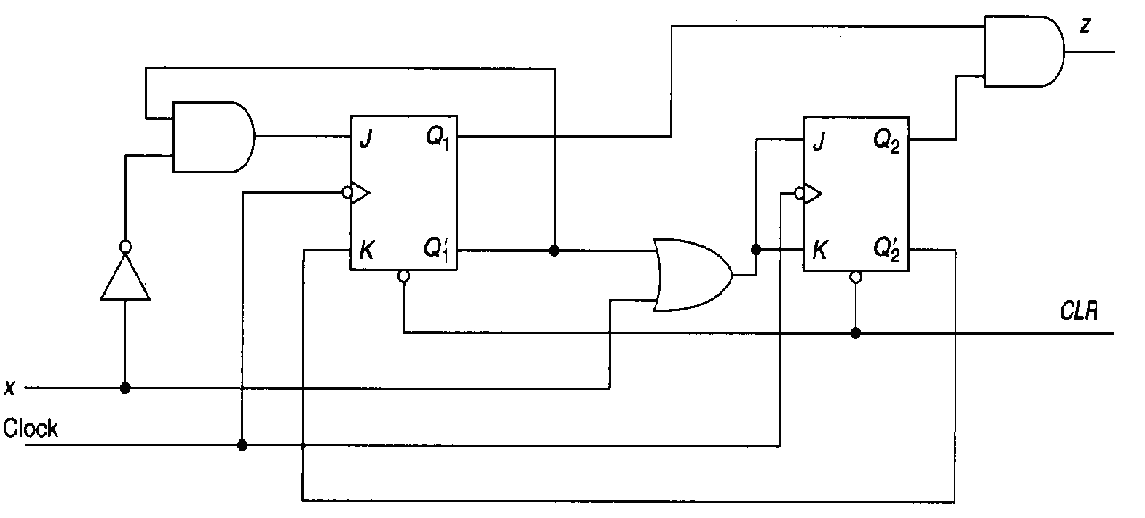
01/0

1. The following boolean function (with its don't cares) is given:

F (A,B,C,D) = Σm (2, 3, 5, 7, 8, 14, 15)

d (A,B,C,D) = Σm (0, 1, 4, 6, 9, 10, 11)

1. Find the most simplified Boolean expression using Karnaugh map simplification method.
2. Draw the combinational circuit for this function using only NAND gates.
3. This function can be implemented by using 4-to-1 multiplexer? Show the circuit if it is possible.
4. Is it possible to implement the function above if we have only 2 X 4 decoders?
5. Perform the following arithmetic operation for binary numbers 10000011 and 00110010 without converting to decimal. The binary numbers listed have a sign in the left most position and, if negative, are in 2’s complement form. Find decimal equivalents of the results.
6. Multiplication ( 16 bits result)
7. Division ( 4 bits result)
8. Using JK flip flops design a counter to produce following sequence: 4 5 3 0 1. *(Give only the expressions for the J and K inputs. No need to draw the circuit.)*
9. Determine the behavior of the circuit in the case of entering unused states.(20)
10. Using JK flip flops design a counter to produce following sequence: 4 0 3 0 1. *(Give only the expressions for the J and K inputs. No need to draw the circuit.)*
11. Determine the behavior of the circuit in the case of entering unused states.(20)
12. What are the differences between an asynchronous counter and a synchronous counter? Which of them is better? Why? (10)
13. Analyze the clocked synchronous state machine below and then draw a state diagram for this state machine (x: input, z:output). (30)
14. Is this machine a Mealy machine or a Moore machine? Explain?
15. Fill in the transition/output table for the above state machine.
16. Draw the Flow Chart for this ASM.



|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Present States | Next States | | Output | |
| X = 0 | X = 1 | X = 0 | X = 1 |
| Q2 Q1 | Q2+ Q1+ | Q2+ Q1+ | Z | Z |
| 0 0 |  |  |  |  |
| 0 1 |  |  |  |  |
| 1 0 |  |  |  |  |
| 1 1 |  |  |  |  |

1. Show the decimal equivalent of two numbers (0101001 1 and 10010101) if they are interpreted as signed Signed-magnitude system, 1’s complement system, 2’s complement system, Gray code or BCD code. (fill the following table by showing calculations for each code or systems)

|  |  |  |
| --- | --- | --- |
|  | 0 1 0 1 0 0 1 1 | 1 0 0 1 0 1 0 1 |
| signed Signed-magnitude system |  |  |
| 1’s complement system |  |  |
| 2’s complement system |  |  |
| Gray code |  |  |
| BCD code |  |  |

1. Design a logic circuit for increment / decrement operation over 4 bit number by usign 4 bit adder. (15)

A : 4 bit number ( A3A2A1A0 )

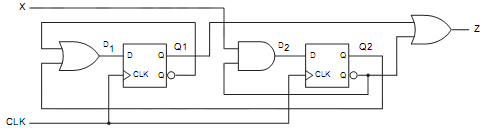
X : control input determining operations

|  |  |  |
| --- | --- | --- |
| X | Operation | |
| 0 | Increment | A + 1 |
| 1 | Decrement | A - 1 |

1. Design a synchronous state machine with the state/output table shown in following table, using D flip-flops. Use two state variables, Q1 Q0 with the state assignment A= 00, B=01, C=11, D=10.
2. Draw the chart. Is it Moore or Mealy type? Explain.(25)

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Present State | Next State | | Output | |
| X=0 | X=1 | X=0 | X=1 |
| A | B | D | 0 | 0 |
| B | C | B | 0 | 0 |
| C | B | A | 1 | 1 |
| D | B | C | 0 | 0 |

1. Analyze the synchronous state machine in the following figure. Write the next state functions ( D1=? D2=?), state table and draw state diagram (use state names A-D for Q1 Q2 = 00 -11).(30)



1. Design a synchronous counter using JK flip flops. The counting sequences is 1 → 0 → 3 while input x equals “0”. When x becomes “1” the sequence is 1→ 3 → 0. Determine the behavior of the circuit for unused states.(30)
2. For the following state diagram, find the corresponding ASM chart and state table. What is the type ?(30)



1. Design a synchronous counter (40)

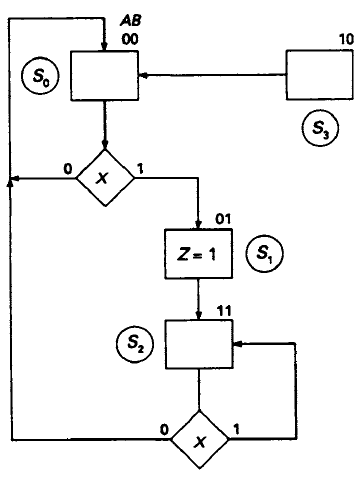
If the input x=1 the counter sequence: 2, 3, 4, 7, 1

If the x=0 the counter sequence : 7 5 1 3 6

1. Design the counter using JK flip flops
2. Test the circuit whether it counts correctly.
3. Determine the behavior of the circuit in the case of entering unused states.
4. Draw Algorithmic State Chart
5. Draw state diagram
6. Design a synchronous counter (25)
7. If the input x=0 the counter sequence: 1,3,0
8. If the x=1 the counter sequence : 2,1,0
9. Design the counter using JK flip flops
10. Determine the behavior of the circuit in the case of entering unused states
11. Draw 3-bits asynchronous down counter. If we need 6 bits one what is the simple circuit?(10)
12. Give the differences between EEPROM and RAM. Which of them is better? Why?(10)
13. A memory has 10 data (input/output) lines and 12 address lines. What is the bit storage capacity?(10)
14. Using Boolean Algebra find the simplest form of the expression (10)

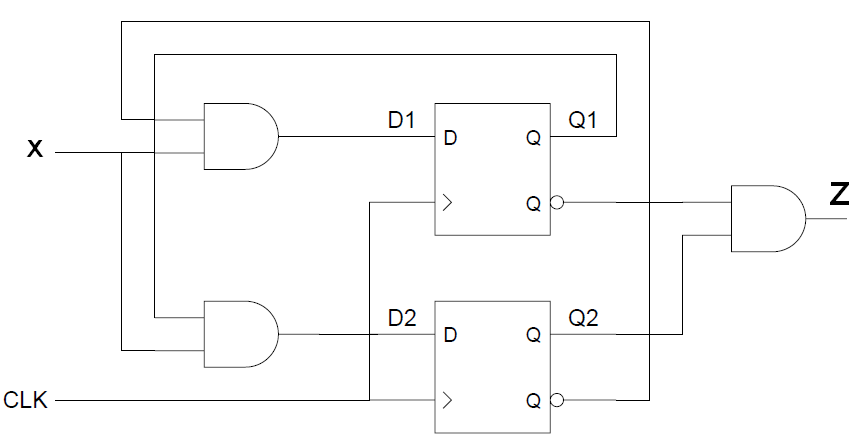


1. Give 3 advantages of digital systems over analog systems(5)
2. For the following ASM chart write the type, the state diagram and state table.(10)



1. Hexadecimal numbers F5 and 7C will be transferred with a parity bit. What is the **odd** parity bit?
2. Design a logic circuit which calculates (Q) multiplication of two numbers (A and B) with two bits(20)

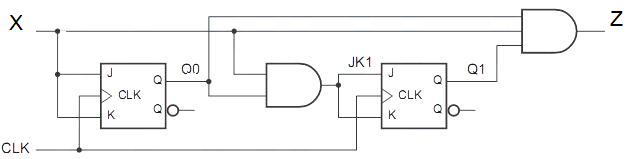
(A1A0) x (B1B0 )= Q3Q2Q1Q0

1. Explain combinational and sequential logic circuits. Write the differences between them.
2. Analyze the clocked synchronous state machine below and then draw a state diagram for this state machine (x: input, z:output).(20)
3. Is this machine a Mealy machine or a Moore machine? Explain?
4. Fill in the transition/output table for the above state machine.
5. Draw the Flow Chart for this ASM.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Present | Next States | | Output | |
| States | X = 0 | X = 1 | X = 0 | X = 1 |
| Q1 Q2 | Q1+ Q2+ | Q1+ Q2+ | Z | Z |
| 0 0 |  |  |  |  |
| 0 1 |  |  |  |  |
| 1 0 |  |  |  |  |
| 1 1 |  |  |  |  |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 1. There is an analog signal changing between 0 and 12 volt. Design a circuit to show the value of the signal on a 7 segments display. Displayed numbers is changed according to the value of the input signal :20 | | | | | | | | | | | | | |
| Analog Signal (volt) | | | 0-2 | | 2-4 | 5-6 | 6-7 | 7-8 | 8-9 | 9-10 | 10-12 |
| Display Value | | | 0 | | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| Transition Table for JK Flip Flop | | | | | | | | |  | | |
| OUTPUT TRANSITION | | FLIP-FLOP INPUTS | | |  | | | | | |
| Qn | Qn+1 | J | | K |  | | | | | | | |
| 0 | 0 | 0 | | X |  | | | | | | | |
| 0 | 1 | 1 | | X |  | | | | | | | |
| 1 | 0 | X | | 1 |  | | | | | | | |
| 1 | 1 | X | | 0 |  | | | | | | | |

1. Analyze the clocked synchronous state machine below and then draw a state diagram for this state machine (x: input, z:output).25
2. Is this machine a Mealy machine or a Moore machine? Explain?
3. Fill in the transition/output table for the above state machine.
4. Draw the Flow Chart for this ASM.



|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Present States | Next States | | Output | |
| X = 0 | X = 1 | X = 0 | X = 1 |
| Q1 Q0 | Q1+ Q0+ | Q1+ Q0+ | Z | Z |
| 0 0 |  |  |  |  |
| 0 1 |  |  |  |  |
| 1 0 |  |  |  |  |
| 1 1 |  |  |  |  |

1. A 4-bit ripple up counter consists of flip-flop that each has a propagation delay from clock to Q output of 16ns. For the counter to recycle from 1110 to 0001, it takes a total of …... ns (10)
2. The following boolean function (with its don't cares) is given:

F (A,B,C,D) = Σm (1, 3, 7, 12, 13)

d (A,B,C,D) = Σm (0, 5, 8, 11)

* 1. Find both minimum sum of products and minimum product of sums expressions using Karnaugh map simplification method.
  2. Draw the combinational circuit for the simplest function using only NAND gates.
  3. This function can be implemented by using 4-to-1 multiplexer? Show the circuit if it is possible.
  4. Is it possible to implement the function above if we have only 2 X 4 decoder ?